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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Hiroshi ISHIYAMA

Group Art Unit: 2814

Application No.: 10/778,029

Examiner: Theresa T. DOAN

Filed: February 17, 2004

Docket No.: 118695

For: SEMICONDUCTOR MODULE HAVING INNER PRESSURE RELEASE PORTION

STATEMENT OF SUBSTANCE OF INTERVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

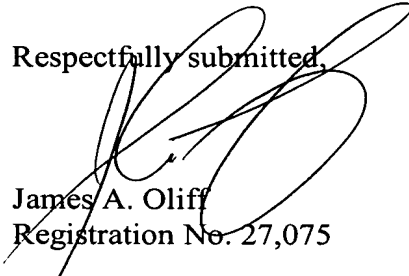
Sir:

A personal interview was conducted on April 4, 2006 between Applicants' representative and Examiner Theresa T. Doan at the U.S. Patent and Trademark Office.

During the interview, the subject matter of this application was reviewed to point out those specific features recited in the rejected claims which distinguish over the applied references. For example, it was asserted that the secondary reference to Fan fails to disclose a first and second electrode plate contacting the first and second surfaces of the semiconductor chip or an inner pressure release portion that extends from the surface of the semiconductor chip to the outside of the resin mold. It was also pointed out that Fan fails to disclose a resin mold that seals a surface of a semiconductor chip and that the alleged inner pressure release portions in Fan fail to extend from the surface of the semiconductor chip, but rather, merely

communicate gap surrounding the chip to the outside. Examiner Doan also indicated that an additional search would be conducted prior to issuance of the next Office Action.

Respectfully submitted,


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JAO:JWF/ldg

Date: April 4, 2006

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